

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

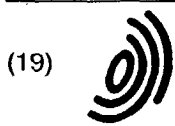
Defects in the images include but are not limited to the items checked:

- ☐ **BLACK BORDERS**
- ☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- ☐ **FADED TEXT OR DRAWING**
- ☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- ☐ **SKewed/SLANTED IMAGES**
- ☐ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- ☐ **GRAY SCALE DOCUMENTS**
- ☐ **LINES OR MARKS ON ORIGINAL DOCUMENT**
- ☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- ☐ **OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.

THIS PAGE BLANK (USPTO)



Europäisches Patentamt
European Patent Office
Office européen des brevets



(11) EP 0 829 808 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
18.03.1998 Bulletin 1998/12

(51) Int. Cl.⁶: G06F 13/38

(21) Application number: 97115949.6

(22) Date of filing: 12.09.1997

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC
NL PT SE

(30) Priority: 13.09.1996 JP 243024/96

(71) Applicant: NEC Corporation
Minato-ku, Tokyo 108-01 (JP)

(72) Inventor:
Horiguchi, Yoshihiro,
NEC IC Microcomp. Syst. Ltd.
Kawasaki-shi, Kanagawa (JP)

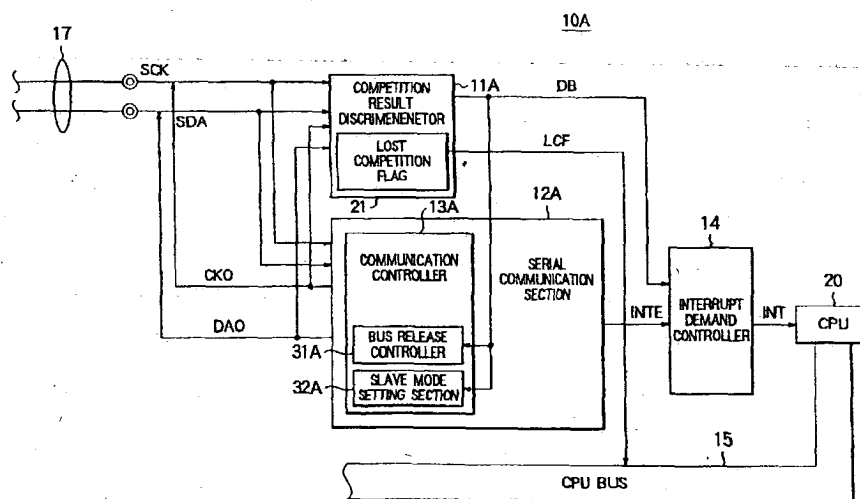
(74) Representative:
Turi, Michael, Dipl.-Phys. et al
Samson & Partner
Widenmayerstrasse 5
80538 München (DE)

(54) Serial bus controller

(57) A serial bus controller comprises a competition result discriminator (11A) for outputting a lost competition signal (DB) upon detecting a lost competition, by comparing a clock SCK and data SDA on a serial communication bus (17) against a clock CKO and data DAO, respectively, to be output from the own station to find any difference between them, a bus release controller (31A) for performing end-of-communication procedures

including releasing the serial communication bus (17) in response to the lost competition signal (DB), and a slave mode setting section (32A) for effecting slave mode setting procedures in response to the lost competition signal (DB) and based on the data SDA on the serial communication bus (17).

FIG. 3



EP 0 829 808 A2

Description

BACKGROUND OF THE PRESENT INVENTION

(a) Field of the present invention

The present invention relates to a serial bus controller used in a microcomputer-applied device for controlling a serial communication bus connected to a plurality of microcomputer-applied devices, any of which is a candidate for the master device on the serial communication bus.

(b) Description of the Related Art

Recently, as a higher level is achieved in the function and performance of the microcomputer-applied devices, the volume of data to be communicated between microcomputer-applied devices, or computer stations, has been increased. This tendency highlights the importance of the performance in data communication between the microcomputer-applied devices, which includes a higher reliability in data communication as well as a higher speed.

Any of the microcomputer-applied devices of this sort itself can be a candidate for the master device on the serial communication bus which plays a leading role in the data communication during a certain interval. In a data communication system including a plurality of such candidates on a single serial communication bus, if which one is the master device and the others are the slave devices are not clear, proper data communication cannot be normally achieved. When a plurality of candidates for the master device simultaneously start communication as the master device, competition takes place among the candidates. In such a circumstance, there is a scheme in the system for selecting one of the candidates as the sole master device by utilizing the interference between the data thus transmitted, which eventually specifies one or more losers in the competition.

The losers in the competition are requested to release the serial communication bus immediately upon losing the competition, not to interfere with the communication effected by the winner in the competition, or master device. Besides, the loser must perform an after-treatment for the failed communication which becomes due as a result of the lost competition, as well as preparation procedures as a slave device possibly assigned by the master device.

Fig. 1 is a block-diagram showing a conventional serial bus controller in a computer station. The conventional serial bus controller 10 for controlling data communication through a serial communication bus 17 comprises a competition result discriminator 11 and a serial communication section 12. The competition result discriminator 11 compares a clock signal SCK and the contents of data SDA appearing on the serial communi-

cation bus 17 against a clock signal CKO and the contents of data DAO, respectively, output from the serial communication section 12 of the own station, to supply a lost competition/interrupt demand signal INTD to a CPU (not shown in the drawing) when the lost competition is detected as a result of the comparison.

The serial communication section 12 comprises a communication controller 13 for controlling the communication through the serial communication bus 17, and generates an end-of-communication/interrupt demand signal INTE after performing normal serial communication procedures. A CPU bus 15 connects the serial bus controller 10 with the CPU for data transmission, whereas an internal bus 16 connects the serial control section 12 with the CPU bus 15. The communication controller 13 comprises a bus release controller 31 and a slave mode setting section 32.

With reference to Fig. 2 showing a time-chart of the conventional serial bus controller 10, additionally to Fig. 1, an example of operations of the conventional serial bus controller 10 will be described, in the event of competition among a plurality of candidates for the master device on the communication bus.

Assume that the serial bus controller 10 of Fig. 1 is in the state of serial data communication (state "M" in Fig. 2), to thereby reveal the own station as one of the candidates for the master device. The competition result discriminator 11 receives the clock signal SCK and the contents of data SDA appearing on the serial communication bus 17, to compare the clock signal SCK and the contents of data SDA with the clock signal CKO and the contents of data DAO, respectively, which are to be output from the own station. The occurrence of the lost competition is decided as a result of the comparison if any difference is recognized in the comparison, and the lost competition/interrupt demand signal INTD is output from the serial communication section 12.

During processing the lost competition interrupt procedures which become due as a result of the lost competition, the CPU provides a command through the internal bus 16 to the bus release controller 31 to halt the output of the clock signal CKO and data DAO from the own station, thereby releasing the communication bus 17 in the procedure "B" in Fig. 2 in order not to interfere with the communication made from the master device, or winner in the competition. Further, the CPU performs an after-treatment for the failed communication which is due as a result of the lost competition, and provides a command to the slave mode setting section 32 to perform communication preparation procedures for a slave device ("C" in Fig. 2) which may be possibly assigned by the master device.

On the other hand, if the communication by the serial bus controller 10 is finished properly as a result of winning in the competition, the serial communication section 12 outputs the end-of-communication/interrupt demand signal INTE, and the CPU provides a command to the serial bus controller 10 to perform end-of-

communication procedures ("D" in Fig. 2) including communication preparation procedures for a slave device which may be possibly assigned by the master device, and to perform preparation procedures for the next communication.

After finishing the above procedures, the serial bus controller 10 which is either in the state of the slave device or in the state of master device moves into an idling state ("RY" in Fig. 2). After the idling state "RY" as a slave device, the serial bus controller 10 works in the state of the master device "M" if the state of the slave device is restored to the state of the master device, or works in the state of slave device "S" if the serial bus controller 10 is assigned as such ("M/S" in Fig. 2). Before arrival at the waiting state "RY" after the lost competition, the serial bus controller 10 must pass through a communication disabled state "V" in Fig. 2, which fact may cause the serial bus controller 10 to delay in responding to a possible assignment for a slave device made by the master device.

As described above, the serial bus controller performs releasing the serial bus and preparation for a slave device in interrupt procedures after detecting the lost competition. In this procedures, the release of the serial bus is sometimes delayed depending on the program processing speed of the CPU or the state of the serial communication bus. Such a delay of the preparation procedures for the slave device and the release of the serial bus causes troubles against the communication from the master device in the serial communication system.

SUMMARY OF THE PRESENT INVENTION

It is an object of the present invention to provide a serial bus controller which can release the communication bus immediately upon detecting the lost competition to thereby avoid the communication troubles, and perform the lost competition procedures in the timing of the normal end-of-communication procedures.

The present invention provides a serial bus controller used in a computer station for controlling serial data communication transmitted through a serial communication bus connected to a plurality of computer stations each constituting a candidate for a master device and a slave device. The serial bus controller comprises a communication controller for outputting a first serial data to reveal the corresponding computer station as a candidate for the master device, a competition result discriminator for comparing the first serial data with second serial data appearing on the serial communication bus to output a lost competition signal upon detecting the difference between the first serial data and the second serial data, and a hardware device including a bus release controller for releasing the serial communication bus in response to the lost competition signal.

In accordance with the present invention, since the hardware device can release the serial communication

bus in response to the lost competition signal without a command from a CPU, delay in releasing the serial communication bus and in shifting into a slave device can be eliminated. Accordingly, communication troubles such as lack of a slave device in the serial data communication system can be avoided.

The above and other objects, features and advantages of the present invention will be more apparent from the following description, referring to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWING

Fig. 1 is a block-diagram of a conventional serial bus controller;

Fig. 2 is a time-chart showing the operation of the serial bus controller of Fig. 1;

Fig. 3 is a block-diagram of a serial bus controller according to an embodiment of the present invention; and

Fig. 4 is an example of a time-chart showing operation of the serial bus controller of Fig. 3;

DESCRIPTION OF THE PREFERRED EMBODIMENT

Now, the present invention is more specifically described with reference to accompanying drawings, wherein similar constituent elements are designated by the same or related reference numerals throughout the drawings.

Referring to Fig. 3 showing a serial bus controller according to an embodiment of the present invention, the serial bus controller, generally designated by 10A, comprises a competition result discriminator 11A for outputting a lost competition signal DB, a serial communication section 12A having a communication controller 13A for controlling the communication through the serial bus 17, and an interrupt demand controller 14 for generating an interrupt demand signal INT in the timing of the end-of-communication signal INTE supplied from the serial communication section 12A. The interrupt demand signal INT is supplied to a CPU 20 for an external interruption which does not include the information of the lost competition.

The competition discriminator 11A has therein a lost competition flag (LCF) 21 which is set at "1" in response to the detected lost competition to notify the CPU 20 of the occurrence of the lost competition. The communication controller 13A has a bus release controller 31A, implemented as a switching section, for releasing the serial communication bus 17 by a hardware configuration in response to the lost competition signal DB without the command from the CPU 20, and a slave mode setting section 32A for effecting slave mode setting procedures in response to the lost competition signal DB.

Referring to Fig. 4, additionally to Fig. 3, an example of operations of the serial bus controller will be

described.

Assume that the serial bus controller 10A is in the state of serial data communication (state "M" in Fig. 4) to reveal itself as one of the candidates for the master device. The competition result discriminator 11A receives a clock signal SCK and the contents of data SDA appearing on the serial communication bus 17, to compare them with a clock signal CKO and the contents of data DAO, respectively, to be output from the own station. If any difference is recognized in the comparison, occurrence of the lost competition is decided in the competition result discriminator 11A, which sets a lost competition flag LCF and generates a lost competition signal DB.

In response to the lost competition signal DB, the bus release controller 31A in the communication controller 13A releases the serial communication bus 17 by cut-off the connection to halt the output of the clock signal CKO and data DAO from the own station, in order not to interfere with the communication from the master device.

Further, the slave mode setting section 32A turns into a slave preparation mode in response to the lost competition signal DB to receive data from the serial communication bus 17 and compare the address specified by the received data against the own address. If a coincidence is detected therebetween, the slave mode setting section 32A knows that the own station is assigned a slave device by the master device, and responds to the master device through the serial communication bus 17. Thus, the serial bus controller 10A can move immediately into a waiting state as the slave device ("RYS" in Fig. 4) without delay, since the communication bus 17 is already released by the hardware configuration upon occurrence of the lost competition without the command from the CPU 20.

An interrupt demand controller 14 receives the lost competition signal DB from the competition result discriminator 11A, and supplies an interrupt demand signal INT to the CPU 20 in the timing of an end-of-communication signal INTE supplied from a serial communication section 12A. In the serial communication system in general, end-of-communication signal is generated at the end of each communication frame. The interrupt demand signal INT is thus supplied to the CPU at this timing.

The slave mode setting section 32A performs an after-treatment "A" in Fig. 4 for the failed communication which becomes due as a result of the lost competition. The after-treatment "A" is conducted during the time interval while the processing for the interrupt demand signal INT is performed in the CPU 20. The after-treatment "A" includes end-of-communication procedures including communication preparation procedures for a slave device which may be possibly requested by the master device, and preparation procedures for the next communication. The CPU 20 knows the lost competition from the lost competition flag LCF before processing for

the interrupt demand signal INT. If the lost competition flag LCF is set, the CPU prepares retransfer of data or other procedures necessitated by the lost competition. On the other hand, if the lost competition flag LCF is not set, a normal end-of-communication is decided in the CPU by receiving the interrupt demand signal INT.

As described above, since the serial bus controller 10A according to the present embodiment has the competition result discriminator which generates the lost competition signal by comparing the serial data appearing on the serial communication bus against the serial data output from the own station, and a hardware device for performing the release of the communication bus in response to the lost competition signal, delay in releasing the serial communication bus can be eliminated, and troubles in the serial data communication from the master device can be avoided.

Further, since it is possible to respond to assignment of a slave device by the master device without delay in the serial bus controller, the communication disabled period caused by lacking a slave device can be avoided.

Furthermore, since the lost competition interrupt is processed in the timing of the normal end-of-communication interrupt, burdens on processing programs, together with the program development burdens, can be reduced.

Since the above embodiments are described only for examples, the present invention is not limited to the above embodiments and various modifications or alterations can be easily made therefrom by those skilled in the art without departing from the scope of the present invention.

Claims

1. A serial bus controller for controlling serial data communication transmitted through a serial communication bus (17) connected to a plurality of computer stations each constituting a candidate for a master device and a slave device, said serial bus controller comprising: a communication controller (13A) for outputting a first serial data to reveal the corresponding computer station as a candidate for the master device; and a competition result discriminator (11A) for comparing said first serial data with second serial data appearing on the serial communication bus (17) to output a lost competition signal (DB) upon detecting the difference between said first serial data and said second serial data; characterized by a hardware device including a bus release controller (31A) for releasing the serial communication bus (17) in response to said lost competition signal (DB).
2. A serial bus controller as defined in claim 1 wherein said hardware device further includes a slave mode setting section (32A) for setting a slave mode in

response to said lost competition signal (DB), wherein said slave mode setting section (32A) sets the own station to a state of the slave device based on said second serial data.

3. A serial bus controller as defined in claim 1 wherein said competition result discriminator (11A) sets a lost competition flag (21) upon detecting the difference between said first serial data and said second serial data.

4. A serial bus controller as defined in claim 1 further comprising an interrupt demand controller (14) for outputting an interrupt demand signal (INT) in a timing of an end-of-communication signal (INTE) after occurrence of said lost competition signal (DB).

FIG. 1
PRIOR ART

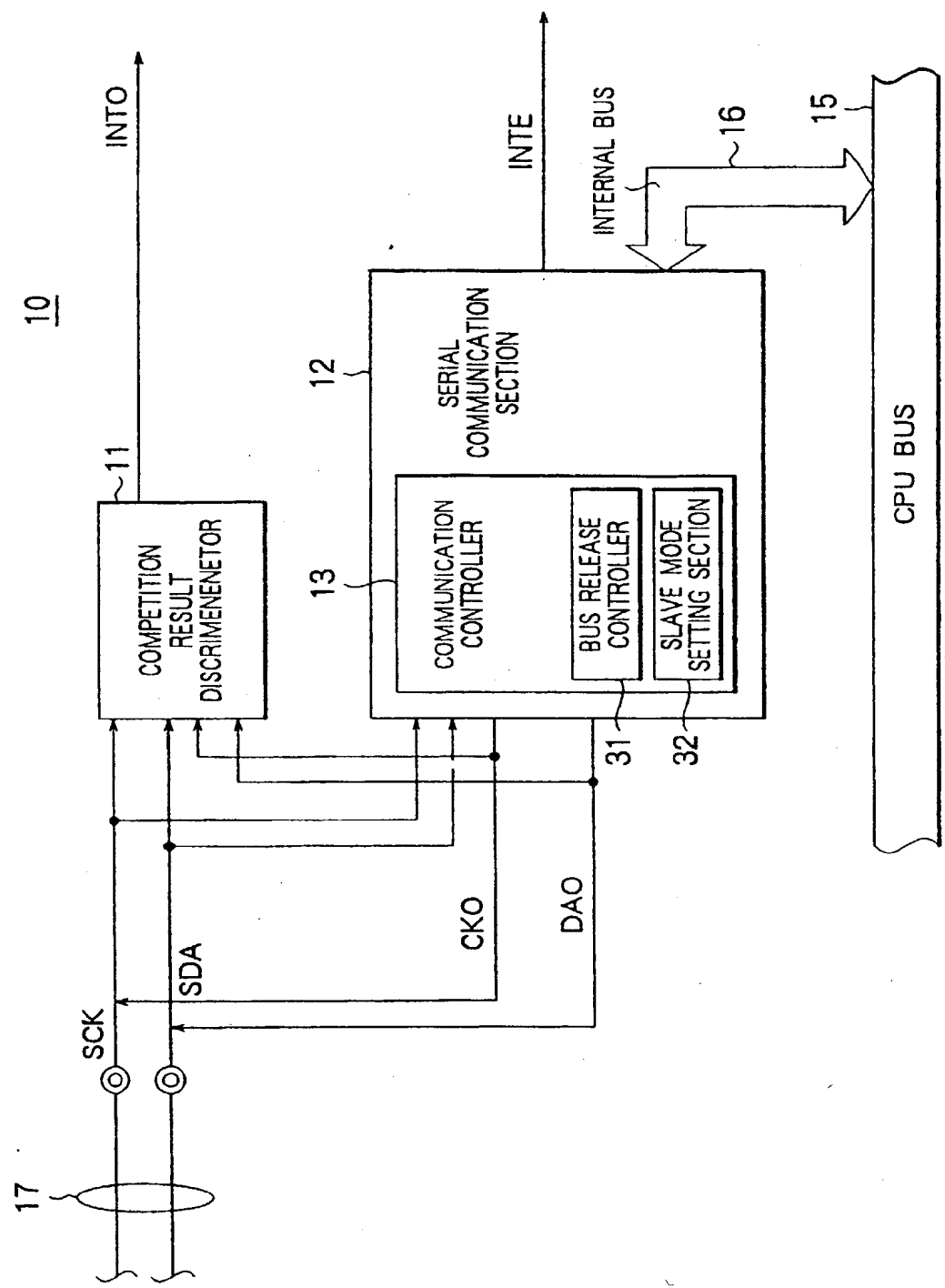


FIG. 2
PRIOR ART

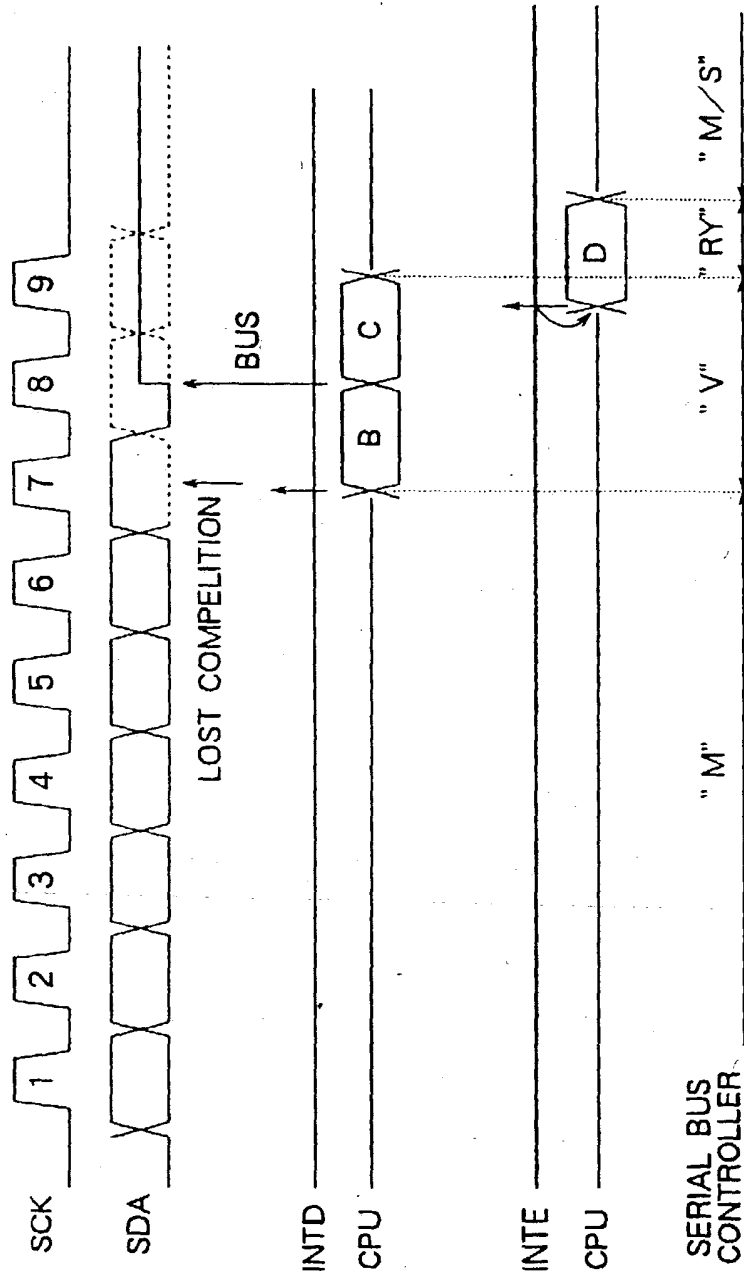


FIG. 3

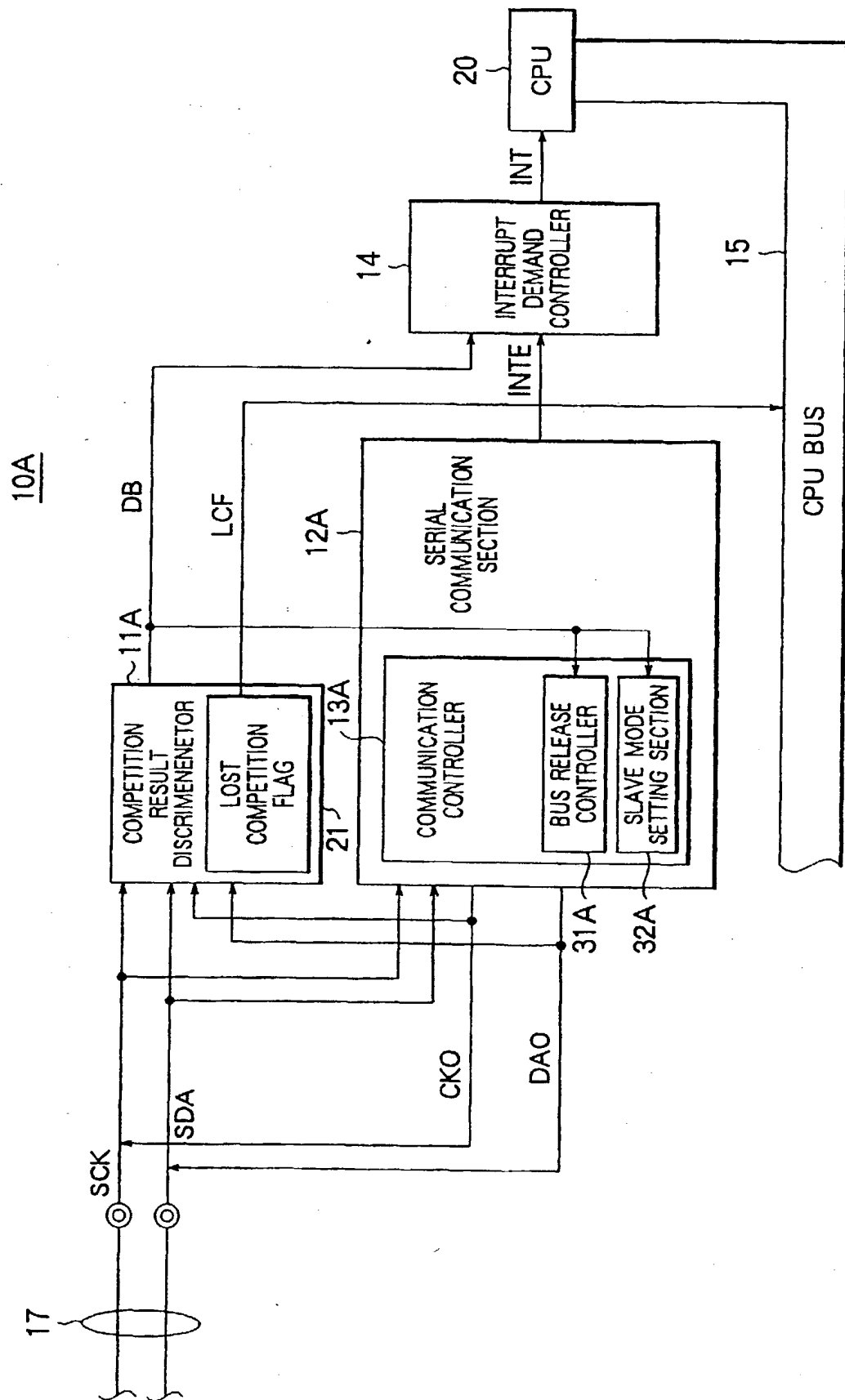
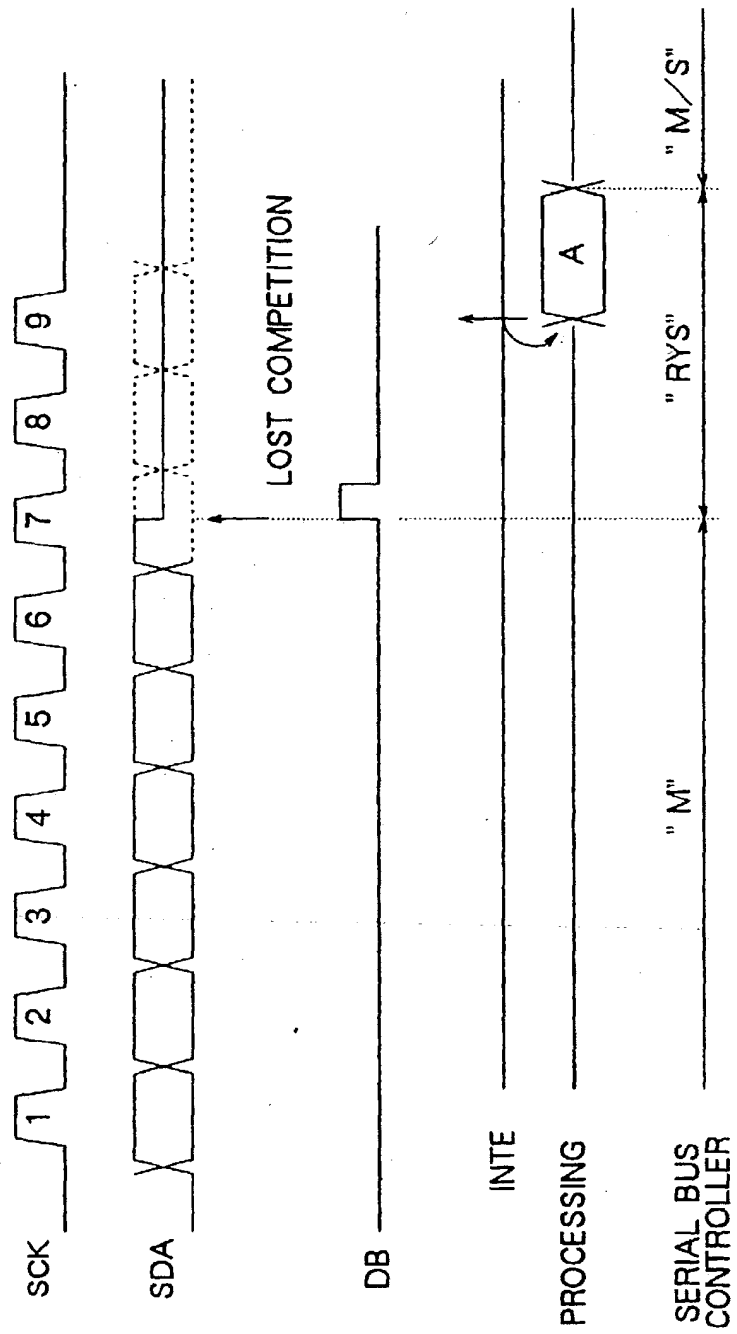


FIG. 4



THIS PAGE BLANK (USPTO)

FIG. 1
PRIOR ART

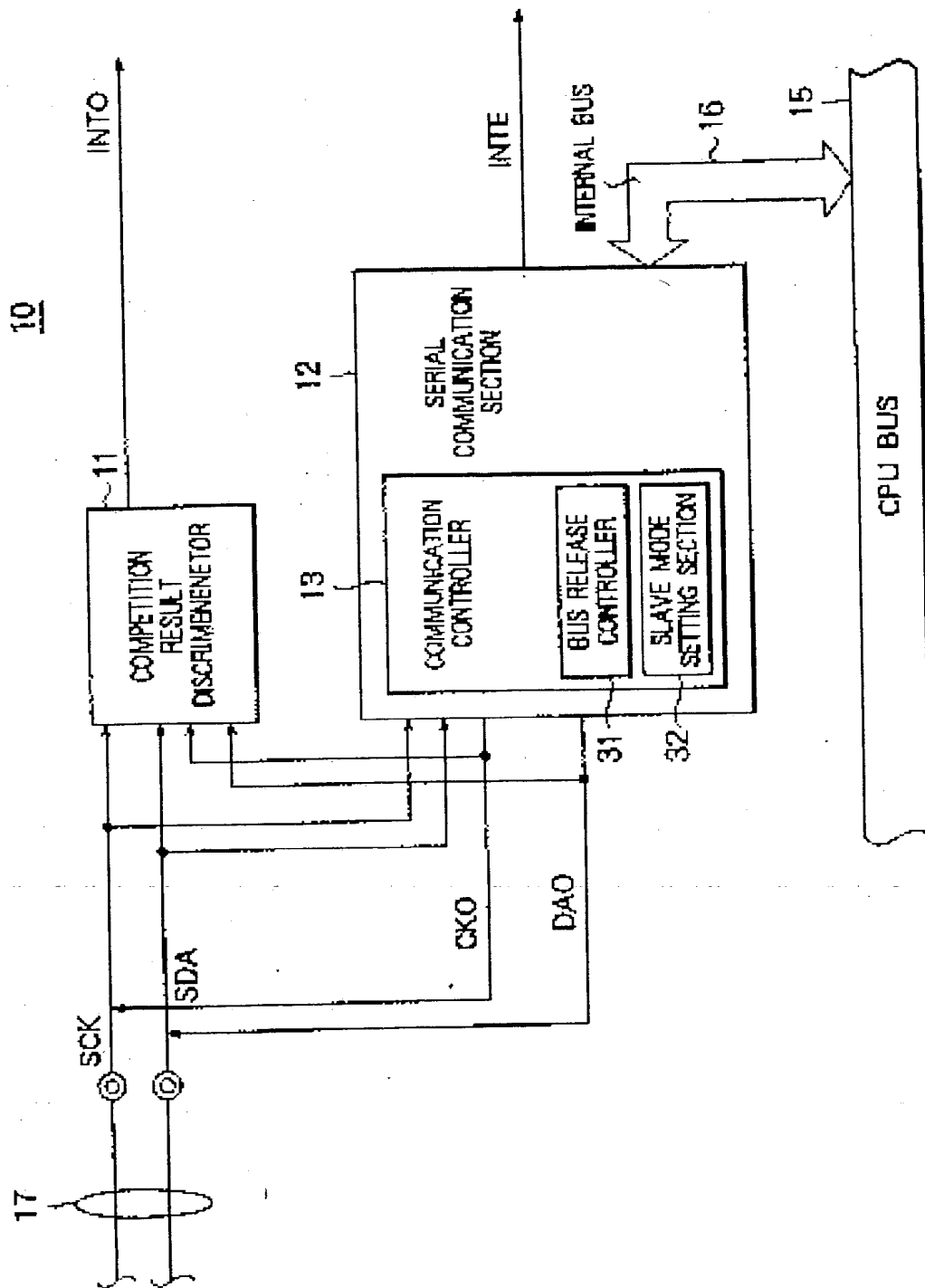


FIG. 2
PRIOR ART

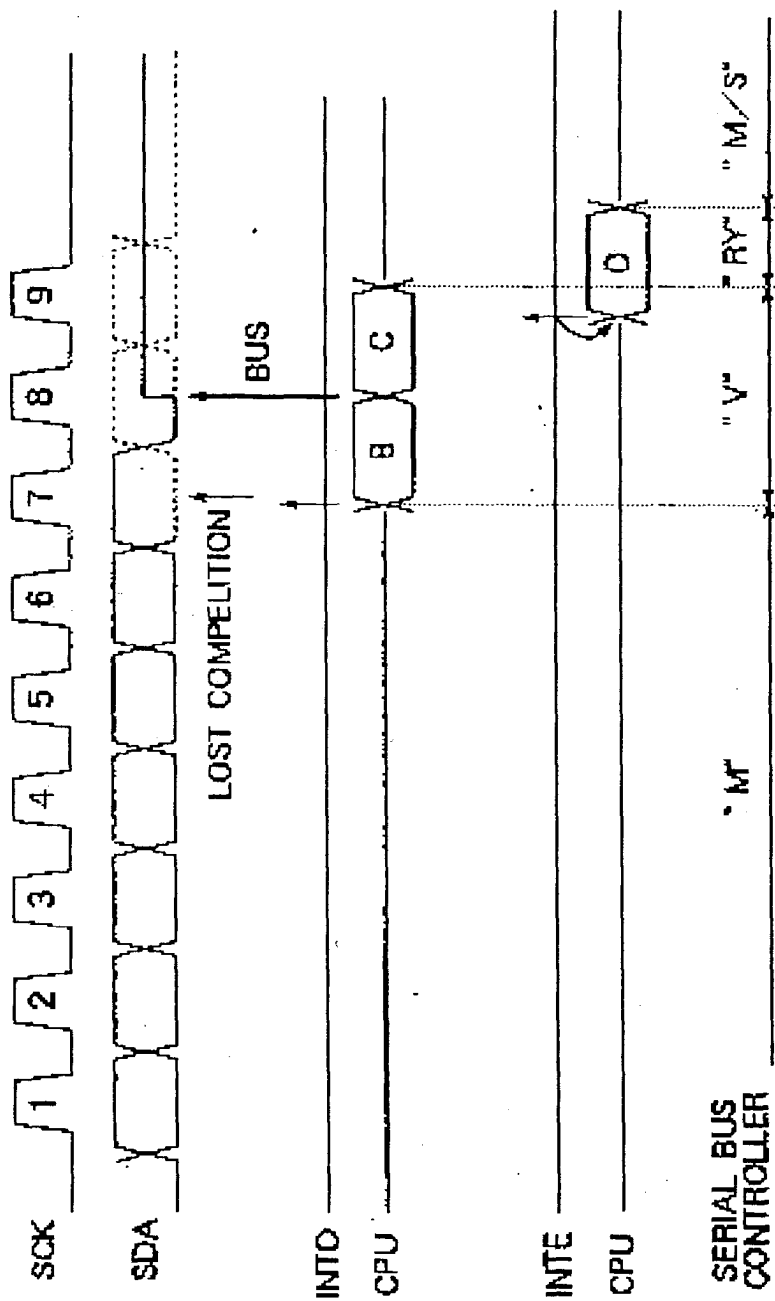


FIG. 3

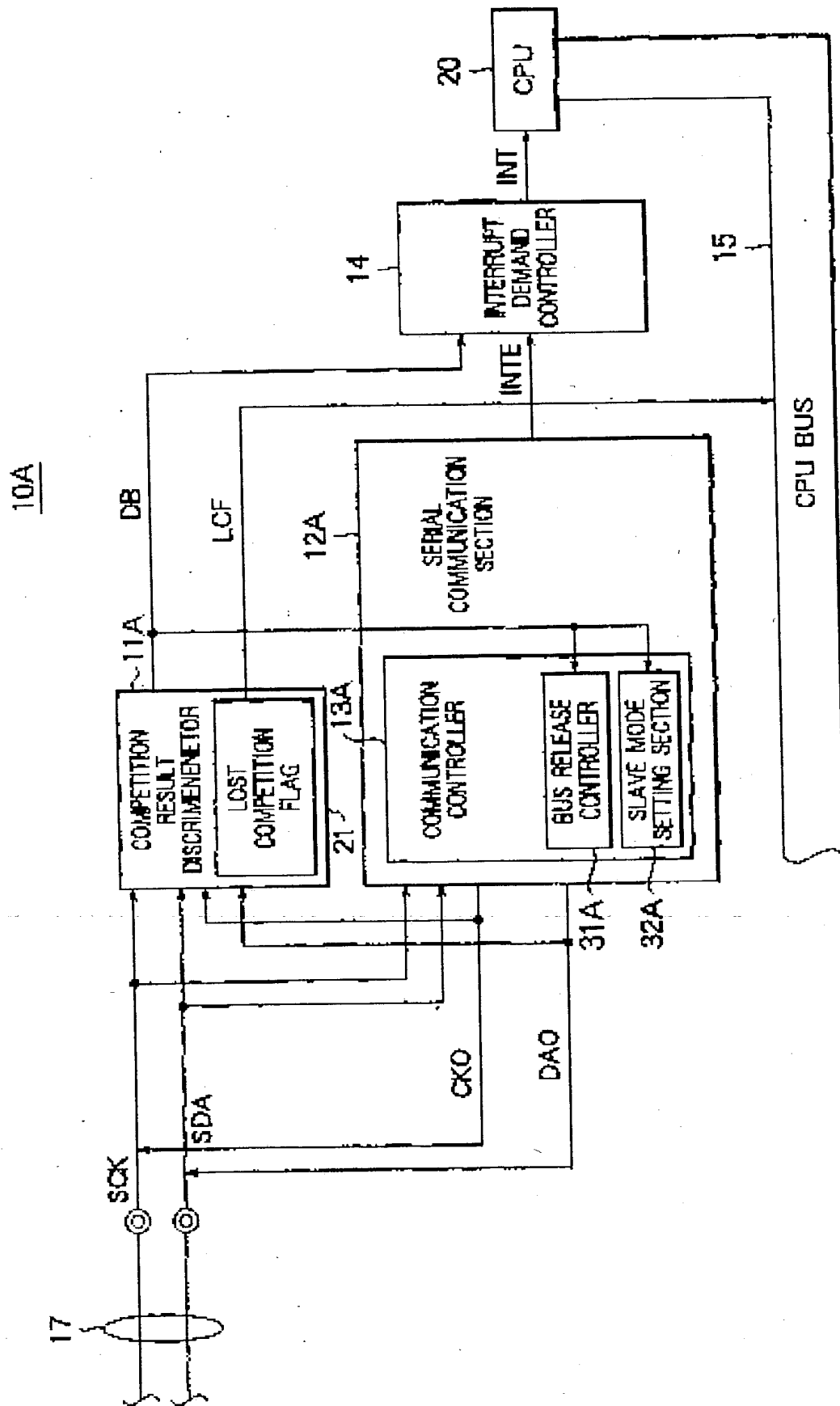
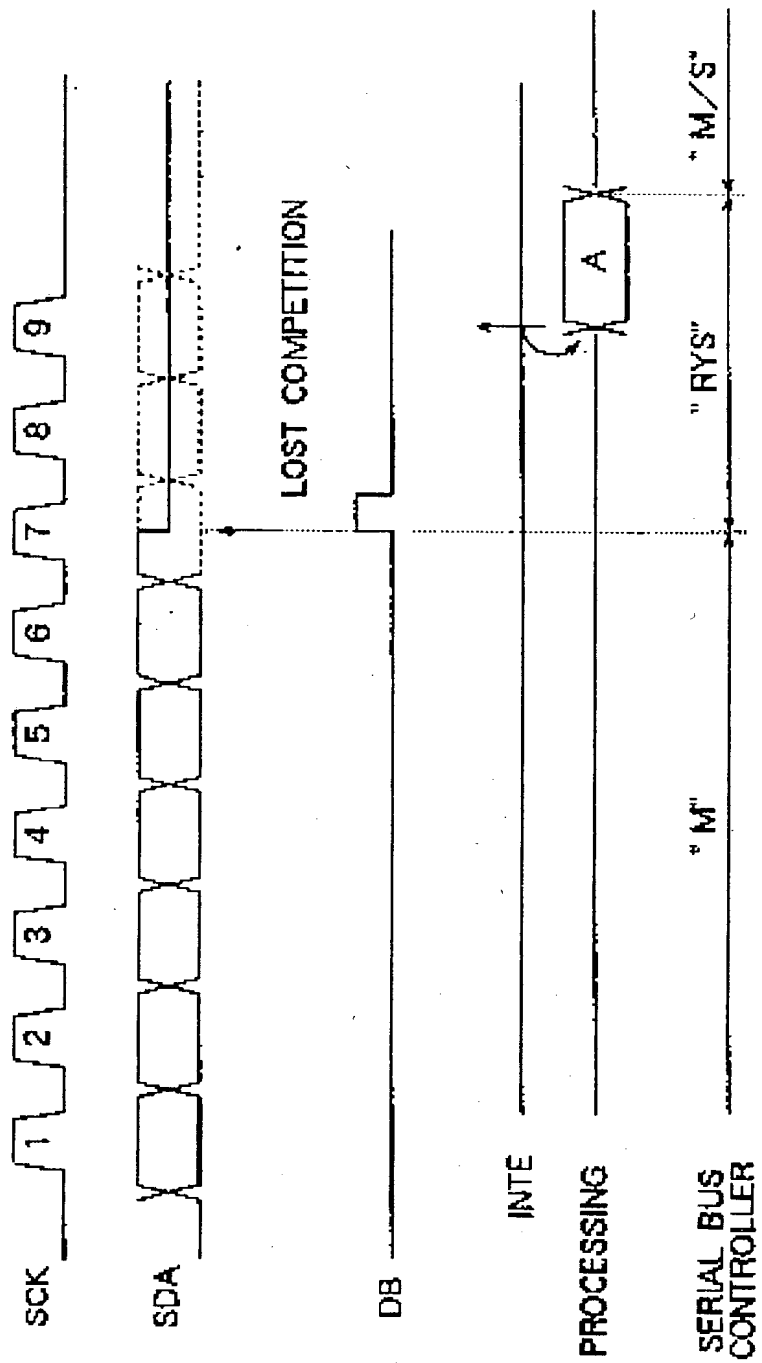
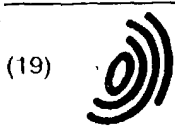


FIG. 4





Europäisches Patentamt
European Patent Office
Office européen des brevets



(11) **EP 0 829 808 A3**

(12)

EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
25.04.2001 Bulletin 2001/17

(51) Int. Cl.⁷: **G06F 13/38**, **G06F 13/42**

(43) Date of publication A2:
18.03.1998 Bulletin 1998/12

(21) Application number: 97115949.6

(22) Date of filing: 12.09.1997

(84) Designated Contracting States:
**AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC
NL PT SE**

(30) Priority: 13.09.1996 JP 24302496

(71) Applicant: **NEC Corporation**
Minato-ku, Tokyo 108-8001 (JP)

(72) Inventor:
Horiguchi, Yoshihiro,
NEC IC Microcomp. Syst. Ltd.
Kawasaki-shi, Kanagawa (JP)

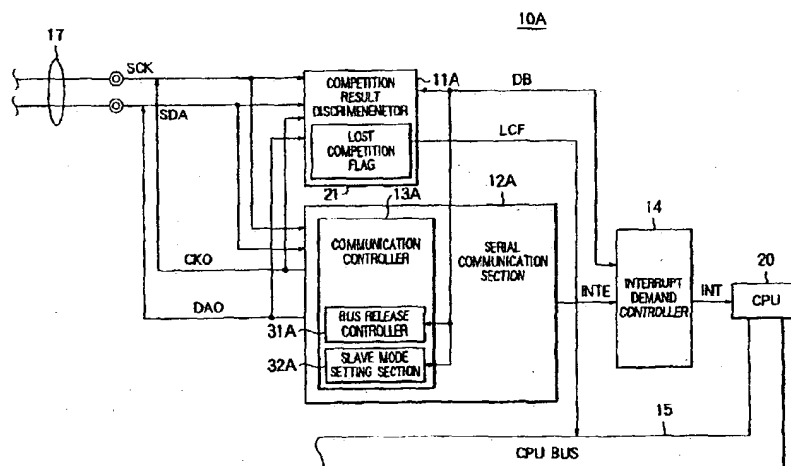
(74) Representative:
Turi, Michael, Dipl.-Phys. et al
Samson & Partner
Widenmayerstrasse 5
80538 München (DE)

(54) Serial bus controller

(57) A serial bus controller comprises a competition result discriminator (11A) for outputting a lost competition signal (DB) upon detecting a lost competition, by comparing a clock SCK and data SDA on a serial communication bus (17) against a clock CKO and data DAO, respectively, to be output from the own station to find any difference between them, a bus release controller (31A) for performing end-of-communication procedures

including releasing the serial communication bus (17) in response to the lost competition signal (DB), and a slave mode setting section (32A) for effecting slave mode setting procedures in response to the lost competition signal (DB) and based on the data SDA on the serial communication bus (17).

FIG. 3



EP 0 829 808 A3



European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 11 5949

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Incl. 6)
Y	US 4 689 740 A (MOELANDS ADRIANUS P M M ET AL) 25 August 1987 (1987-08-25) * column 6, line 46 - column 7, line 14; figures 6, 7 * * column 9, line 9 - line 12 * * column 10, line 56 - line 60. *	1-3	G06F13/38 G06F13/42
Y	MITCHELL R L: "I2C TRANSMISSION TECHNIQUES" WESCON TECHNICAL PAPERS, US, WESTERN PERIODICALS CO. NORTH HOLLYWOOD, vol. 30, 18 November 1986 (1986-11-18), pages 21-2-1-21-2-08, XP000810862 * page 4, right-hand column; figure 4 *	1-3	
A	US 4 511 895 A (MILLER EDWARD B ET AL) 16 April 1985 (1985-04-16) * column 7, line 50 - column 8, line 22 * * claim 12 *	1-4	
A	US 4 750 176 A (VAN VELDHUIZEN EVERT D) 7 June 1988 (1988-06-07) * column 6 *	1-4	TECHNICAL FIELDS SEARCHED (Int. Cl. 6) G06F
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 5 March 2001	Examiner Henneman, P
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			

EPO FORM 1503 03/82 (P/C/C/1)

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 97 11 5949

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

05-03-2001

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4689740 A	25-08-1987	NL 8005976 A	17-05-1982
		AT 7086 T	15-04-1984
		AU 546567 B	05-09-1985
		AU 7699581 A	06-05-1982
		CA 1194574 A	01-10-1985
		DE 3163103 D	17-05-1984
		EP 0051332 A	12-05-1982
		HK 40385 A	31-05-1985
		JP 1710326 C	11-11-1992
		JP 3019740 B	15-03-1991
		JP 63288537 A	25-11-1988
		JP 1663702 C	19-05-1992
		JP 3019741 B	15-03-1991
		JP 63288538 A	25-11-1988
		JP 1520229 C	29-09-1989
		JP 57106262 A	02-07-1982
		JP 63065178 B	14-12-1988
		KR 8801017 B	13-06-1988
		SG 52184 G	29-03-1985
US 4511895 A	16-04-1985	AT 12995 T	15-05-1985
		AU 532683 B	06-10-1983
		AU 6576280 A	22-05-1981
		BR 8008842 A	01-09-1981
		CA 1198160 A	17-12-1985
		DE 3039666 A	14-05-1981
		DE 3070558 D	30-05-1985
		EP 0038852 A	04-11-1981
		JP 56082906 A	07-07-1981
		MY 25886 A	31-12-1986
		WO 8101350 A	14-05-1981
		US 4396844 A	02-08-1983
		US 4489385 A	18-12-1984
		US 4535332 A	13-08-1985
		US 4484258 A	20-11-1984
		US 4367414 A	04-01-1983
		US 4598286 A	01-07-1986
		US 4656475 A	07-04-1987
US 4750176 A	07-06-1988	JP 63014536 A	21-01-1988

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

THIS PAGE BLANK (USPTO)

FIG. 1
PRIOR ART

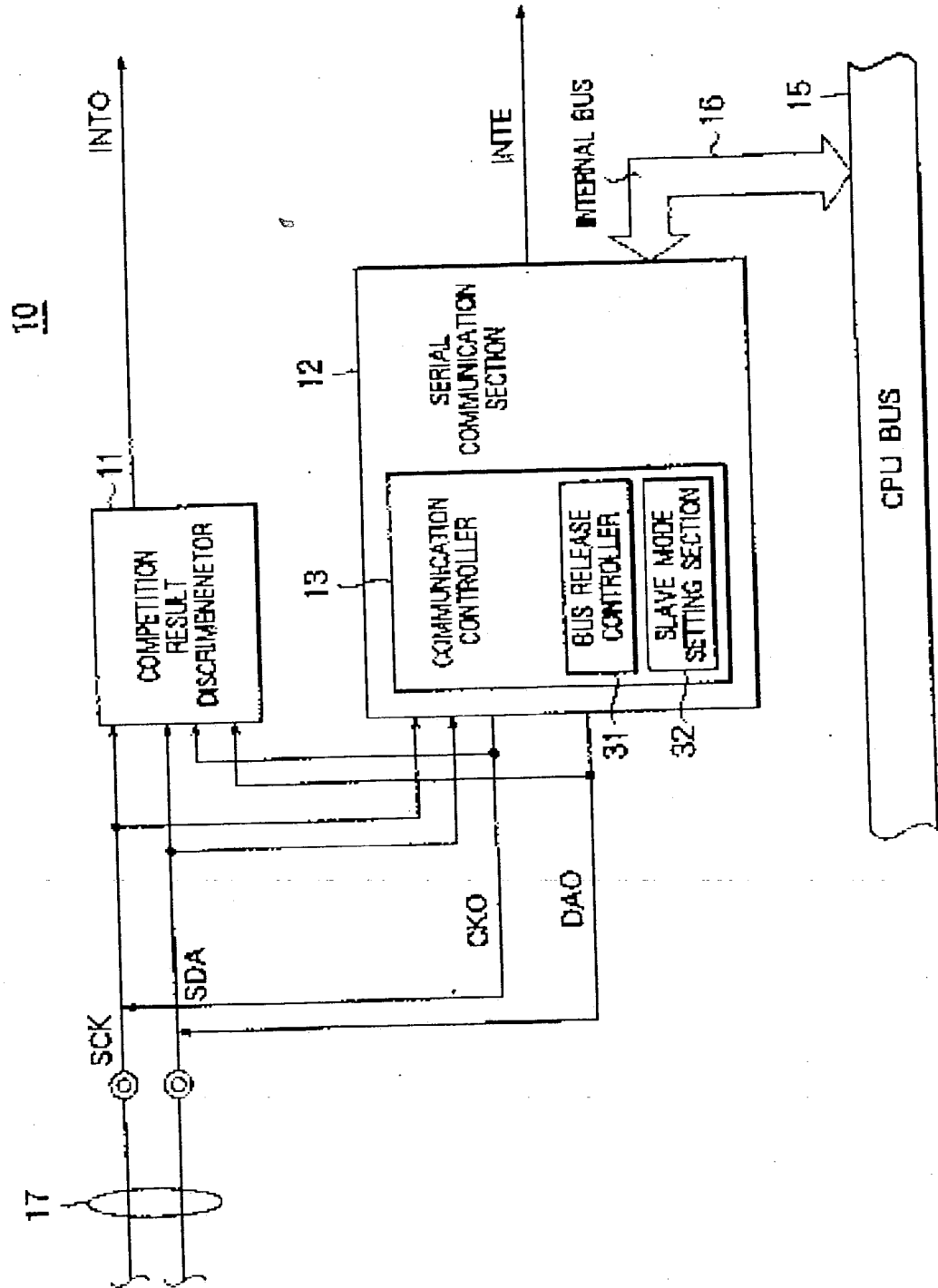


FIG. 2
PRIOR ART

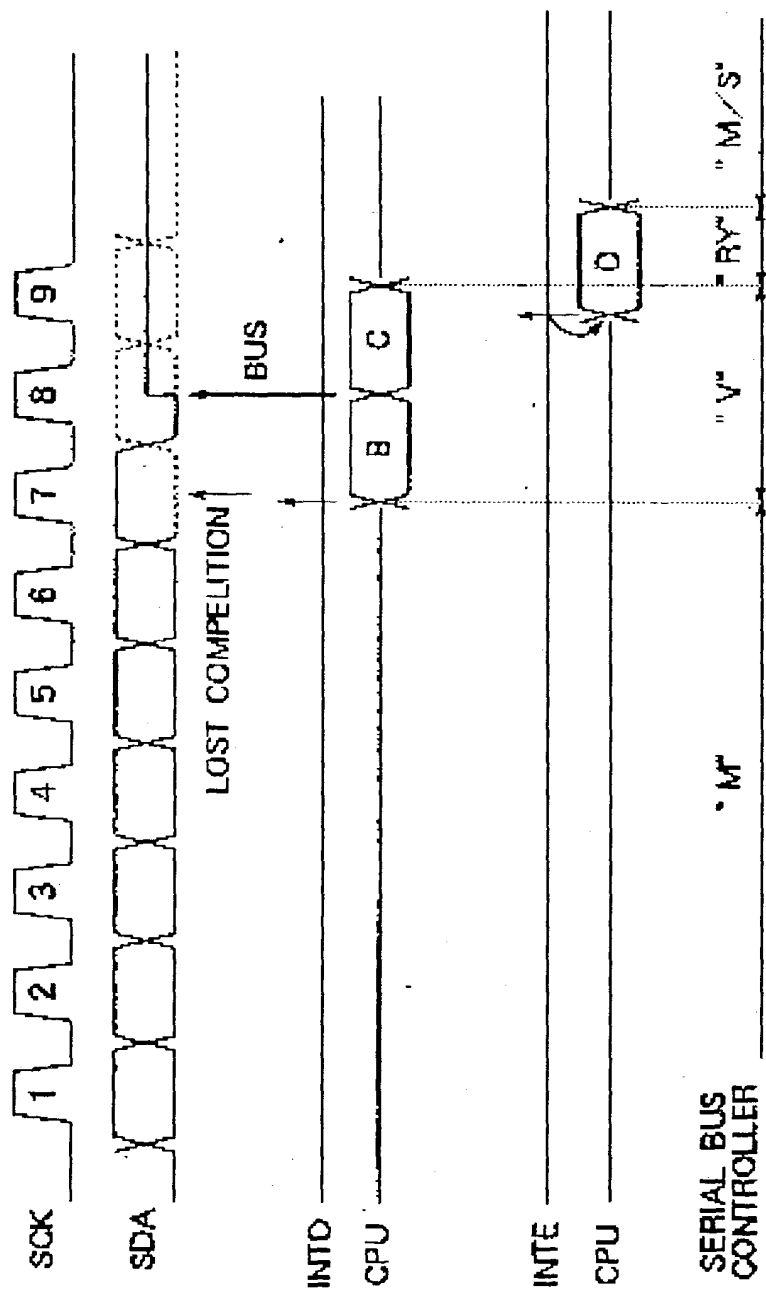


FIG. 3

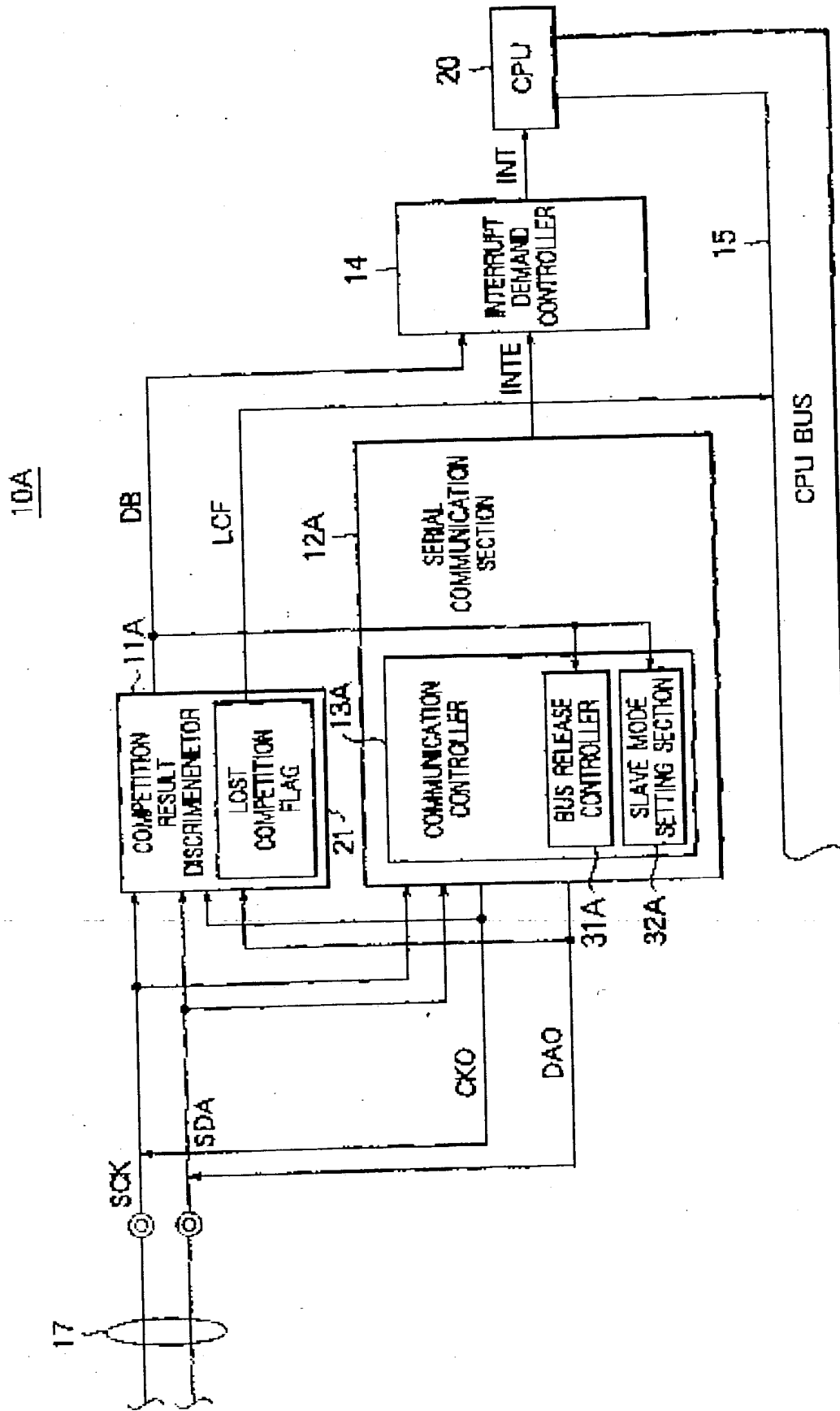


FIG. 4

